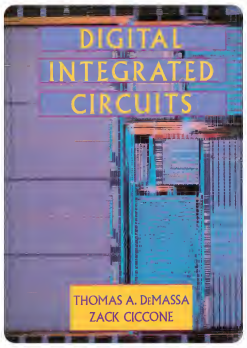
Properties & definitions of Digital ICs



Basic logic operations

NOT AND OR NAND NOR

Gate: A circuit performs a logic function.

Combinational Gates:
Logic Gates performs one or more of Basic operations.

Positive voltage logic

binary 0 (Low voltage)

binary 1 (High voltage)

Inverter:

Non-Inverter (Buffer)

Regenerate voltage levels

* Making degraded high levels higher
* " " low " lower

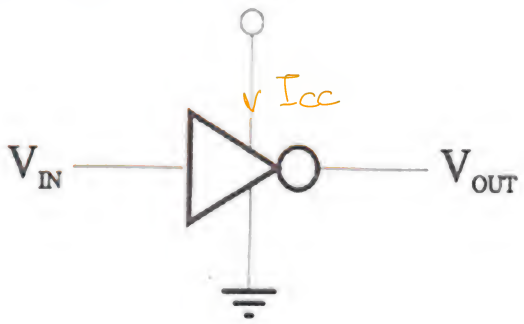
Ideal Logic elements

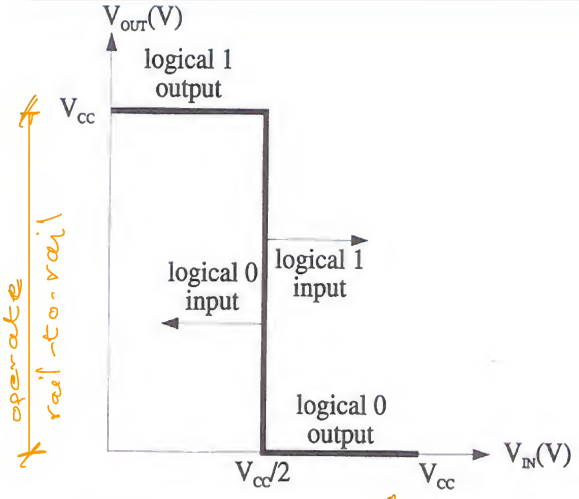
Ideal $I_{cc} = 0$

$P_{cc} = I_{cc} V_{cc}$

Ideal $P_{cc} = 0$

Typically 5V → V_{cc}





Voltage transfer characteristics (VTC)

input 0:

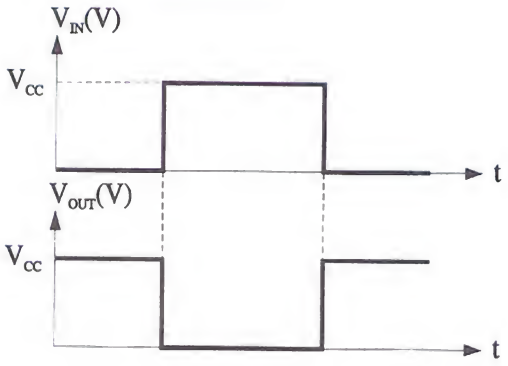
voltage range $0 \leq V_{IN} < V_{cc}/2$

input 1:

voltage range $V_{cc}/2 < V_{IN} \leq V_{cc}$

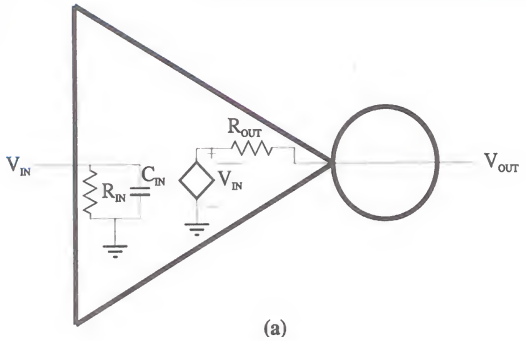
$V_{IN} = V_{cc}/2$ has undefined output & will cause unpredictable results and is therefore avoided

Ideal Transient Characteristics

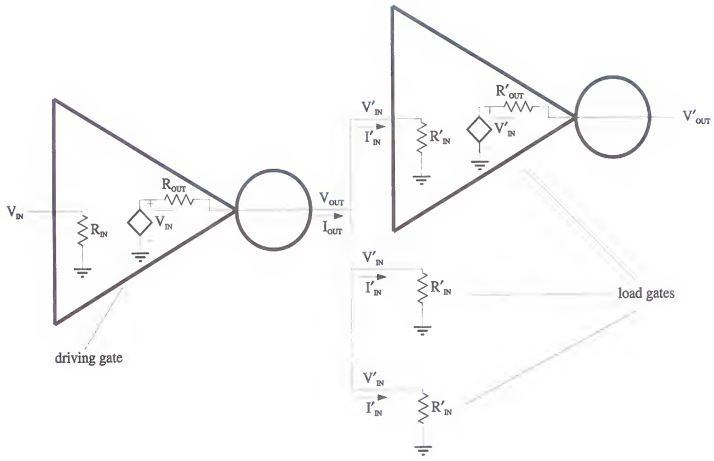


Ideal Input & Output gate impedances

Model of input & output impedance of a logic inverter



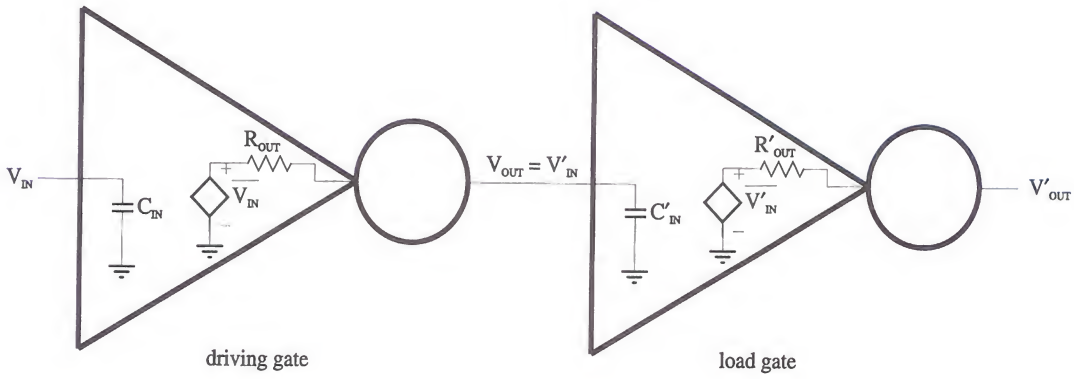
(a)



* The driving gate must provide enough output current to drive all the load gates

$$I_{out} = N I'_{IN}$$

* Ideally an infinite input resistance is desired giving infinite driving capability.



* Faster switching time suggesting an ideal zero output resistance
* Smaller input capacitance will speed up switching time
* Infinit input resistance provide higher charging current for input capacitance

Inverter voltage transfer characteristic (VTC)

A most

$V_{OH} > V_{IH}$

and

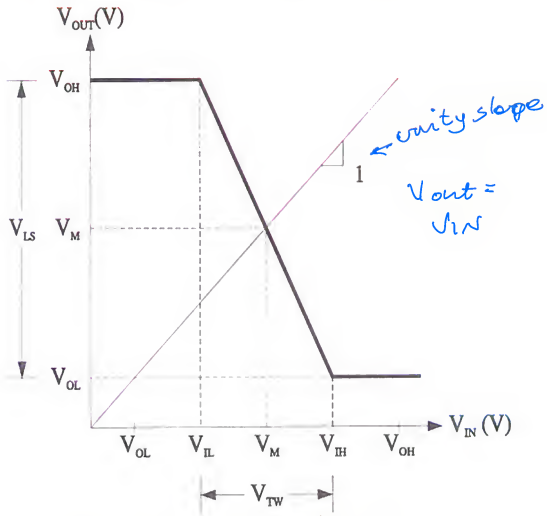
$V_{IL} > V_{OL}$

For design we use worst case values of:

$V_{OH}, V_{OL}, V_{IH}, V_{IL}$

V_M : Midpoint voltage

V_{th} : threshold voltage.

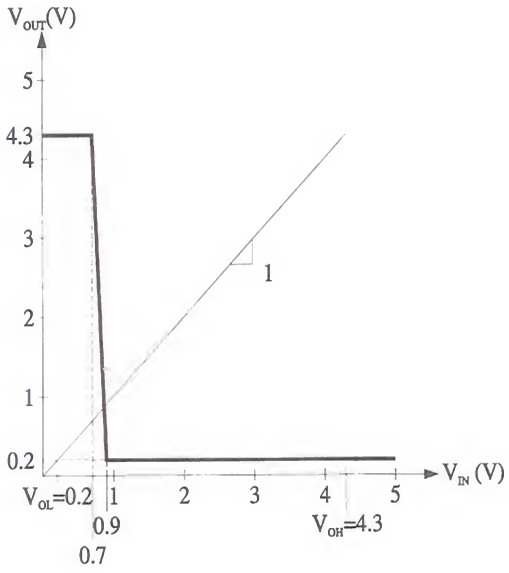


Inverter VTC

V_M is the point on VTC where $V_{out} = V_{IN}$

Example 1.1 ***Voltage Transfer Characteristic Critical Points***

What are the critical voltages V_{OH}, V_{OL}, V_{IL}, V_{IH}, and V_M for the voltage transfer characteristic of Figure



solution:

$V_{OH} = 4.3V$ $V_{OL} = 0.2V$

$V_{IH} = 0.9V$ $V_{IL} = 0.7V$

$V_M \simeq 0.9V$

Logic swing & transition width

LS is the magnitude difference between the output high & low voltage levels

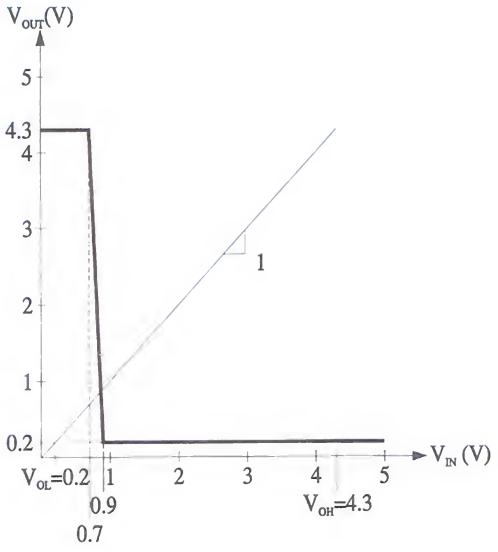
$$V_{LS} = V_{OH} - V_{OL}$$

TW is the amount of voltage change that is required of the input voltage to cause a change in the output voltage from high to low or vice-versa.

$$V_{TW} = V_{IH} - V_{IL}$$

Example 1.2 ***Logic Swing and Transition Width***

Determine the logic swing and transition width for the VTC of Figure



Noise in digital circuits

Noise is variations in steady state voltage levels of digital circuits

* Noise AKA voltage level degradation

Noise Margin

* The voltage noise margins represent a safety margin for the high & low voltage levels.

$$V_{NMH} = V_{OH} - V_{IH} \qquad V_{NML} = V_{IL} - V_{OL}$$

* V_{NMH} & V_{NML} most be positive.

Noise Sensitivities

* The effects of input variations (on the output)

$$V_{NSH} = V_{OH} - V_M \qquad V_{NSL} = V_M - V_{OL}$$

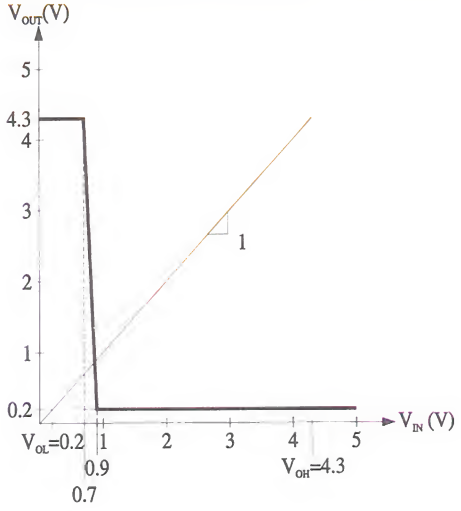
Noise Immunities

* The quantity noise immunity is the ability of a gate to reject noise

$$V_{NIH} = \frac{V_{NSH}}{V_{LS}} \qquad V_{NIL} = \frac{V_{NSL}}{V_{LS}}$$

Example 1.3 ***Noise Margins, Noise Sensitivities and Noise Immunities***

Determine the noise margins, noise sensitivities, and noise immunities for the VTC displayed in Figure



Fan-In & Fan-out

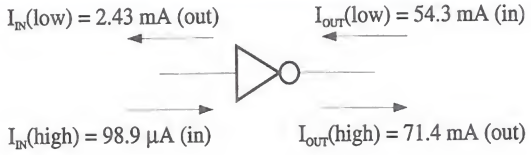
Fan-In The number of the inputs of a gate

Fan-out The " " " outputs of a gate.

$$N_{high} = \frac{I_{out(high)}}{I_{in(high)}} \qquad N_{low} = \frac{I_{out(low)}}{I_{in(low)}} \qquad N_{out} = \min(N_{low}, N_{high})$$

Example 1.4 ***Maximum Fan-Out***

The inverter of Figure 1.7 has the terminal currents $I_{IN}(low) = 2.43$ mA (out), $I_{IN}(high) = 98.9$ μA (in), $I_{OUT}(low) = 54.3$ mA (in), and $I_{OUT}(high) = 71.4$ mA (out). What is the maximum fan-out?

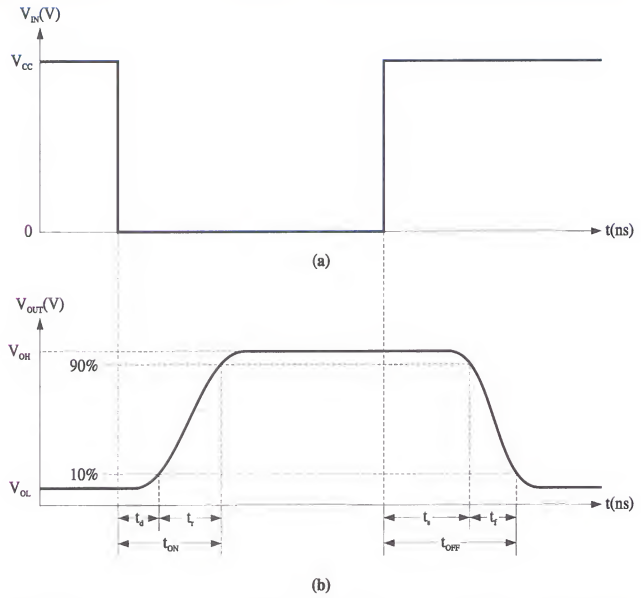


Transient characteristics

* switching voltages from high to low or low to high requires a finit amount of time.
* Propagation delay is the time delay between the change in input voltage & the output voltage response.
* BJT's requires time to store & remove charge from base region
* The transient characteristics of digital circuits employing MOSFET's are limited by the gate oxide capacitance.

Switching Speed definitions

* $t_d \equiv$ delay time
* $t_r \equiv$ raise time
* $t_s \equiv$ storage time
* $t_f \equiv$ fall time
* $t_{ON} \equiv$ turn on time $= t_d + t_r$
* $t_{OFF} \equiv$ turn off time $= t_s + t_f$
* t_r & t_f are the times associates with charging & discharging load capacitance.
* t_s & t_s are associated with stored charge of PN junctions



Switching Speed Definitions: (a) Input pulse, (b) Output pulse

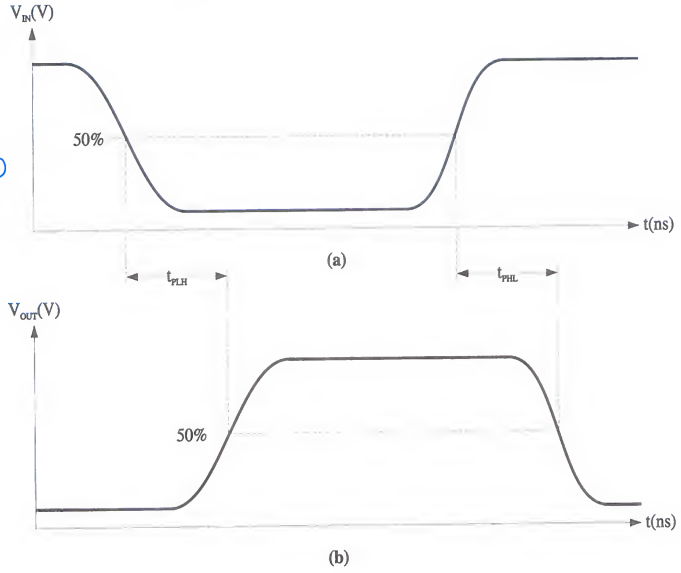
Propagations delays

* The 50% points are used to define the time required for the output to respond to the input.

* t_{PLH} = the low to high propagation delay time

* t_{PHL} = the high to low propagation delay time

* $t_{p(avg)} = \frac{t_{PLH} + t_{PHL}}{2}$



Example 1.5 ***Transient Characteristics***

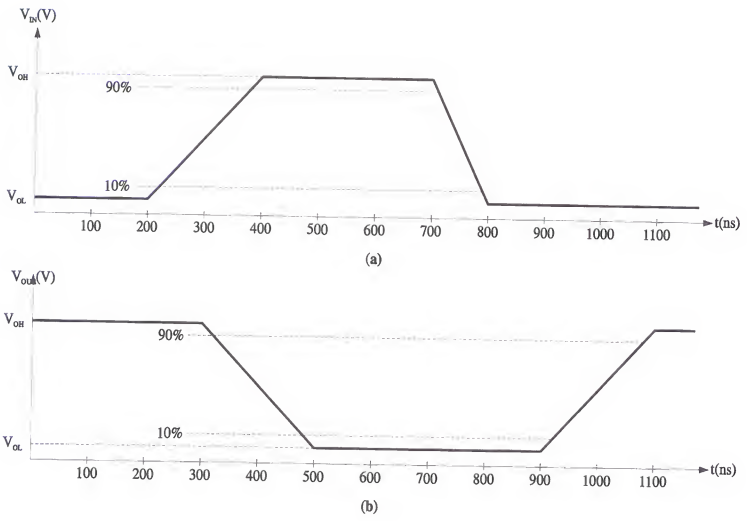
For the input and output waveforms of Figure determine

(a) the switching times t_r and t_f

(b) the propagation delay times t_{PLH} and t_{PHL}.

$t_r = t_f = 168\,ns$

$t_{PHL} = 100\,ns$ $t_{PLH} = 250\,ns$



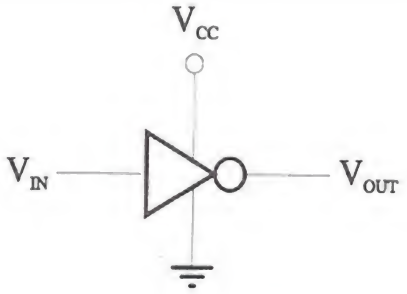
Power Dissipation

$P_{CC(OH)}$

$P_{CC(OL)}$

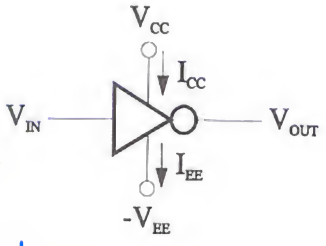
$$P_{CC(avg)} = \frac{P_{CC(OH)} + P_{CC(OL)}}{2}$$

$$P_{CC(avg)} = \left(\frac{I_{CC(OH)} + I_{CC(OL)}}{2}\right) V_{CC}$$



$$P_{Diss(avg)} = P_{CC(avg)} + P_{EE(avg)}$$

$$= \left(\frac{I_{CC(OH)} + I_{CC(OL)}}{2}\right) V_{CC} + \left(\frac{I_{EE(OH)} + I_{EE(OL)}}{2}\right) V_{EE}$$



$P_{CC} = I_{CC} V_{CC}$

$P_{EE} = I_{EE} V_{EE}$

$P_{CC} = I_{CC} V_{CC}$, $P_{EE} = I_{EE} V_{EE}$

Note: P_{EE} = positive power dissipation

Example 1.6 ***Average Power Dissipation***

Determine the average power dissipation for a gate supplied by a 5 V power supply with I(OH) = 1 mA and I(OL) = 3.18 mA.

Power-delay products.

* Low power dissipation and short propagation delay times are both desirable for digital logic circuits.
* Faster propagation delay times are archived at the cost of increased power dissipation
* $P_{diss}(avg) \propto \frac{1}{t_p(avg)}$
* power-delay product: $PD = P_{DISS}(avg)\, t_p(avg)$
* power-delay product ≡ speed-power product
* For Ideal gate $PD = 0$

Example 1.7 ***Power-Delay Product***

The gate of example 1.6 has propagation delay times of t_{PHL} = 1.4 ns and t_{PLH} = 3.2 ns. Calculate the power-delay product for this gate.